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Appln. No.: 09/830,036

Amendment Dated

Reply to Office Action of October 21, 2003

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### FOR EXAMINER REVIEW ONLY

## Remarks/Arguments:

Claims 1, 3, and 12-17 have been rejected under 35 USC §103(a) as being unpatentable over Kusuda et al. (US 5,814,841) in view of Uchida (US 5,751,753) and Ek et al. (US 5,461,243). Claim 5 is allowed. It is respectfully submitted that the rejection of claims 1, 3, and 12-17, as amended, as being unpatentable over Kusuda et al. in view of Uchida and Ek et al. is traversed for the reasons set forth below.

Kusuda et al. disclose laser thyristor structures in Figures 31 and 32 and in the specification at column 22, lines 12-44. These structures include an n-type GaAs substrate (19) with an n-type AlGaAs layer (25), a p-type AlGaAs layer (24), an intrinsic GaAs layer (23), another n-type AlGaAs layer (22), and another p-type AlGaAs layer (21) stacked in order on top of it. The intrinsic GaAs layer (23) functions as the active layer of these laser structures. The specification also discloses that a buffer layer (not shown in the Figures) may be formed between the substrate (19) and the first n-type AlGaAs layer (25).

Uchida discloses a semiconductor laser structure in which a "...buffer layer including a composition graded layer [may be used for] gradually changing the lattice constant..." between the substrate and the clad layer of the structure (Abstract, lines 7-11). Uchida's graded layer is formed from InGaAs (see col. 4, lines 31-37),

Ek et al. disclose that the conventional practice to produce a relaxed SiGe buffer layer on a Si substrate is "...to grow a uniform, graded, or stepped SiGe layer to beyond a metastable critical thickness..." (Column 1, lines 39-41). This relaxed SiGe buffer layer is then used as a surface for growing strained Si layers as part of high mobility structures for FET applications (Column 1, lines 14-17).

The present invention, as recited in claim 1, contains a feature which is neither disclosed, nor suggested by the Kusuda et al., Uchida and Ek et al., singly or in combination, namely:

... four layers consisting of a first conductivity type of AlGaAs layer and a second conductivity type of AlGaAs layer stacked alternately on the buffer layer;

wherein the AlGaAs layer just above the buffer layer is composed of a plurality of AlGaAs layers. Al compositions thereof being increased upward in steps. (Emphasis Added)

This feature, which is illustrated as layers 50-1, 50-2, 50-3, and 50-4 in Figure 6 of the present application, is neither disclosed nor suggested by Kusuda et al., Uchida, Ek or their combination. Uchida specifically teaches to include a composition graded layer as part of the buffer layer and teaches away from including such a composition graded layer in an upper level semiconductor layer (for example, in the clad layer) due to the cross hatch step pattern formed

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in the composition graded layer (column 4, line 64, through column 5, line 9). Ek et al., in the background of their patent, disclose the use of a buffer layer stepped composition SiGe buffer layer on which to grow strained Si layers, but do not suggest the use of such structures in layers above the buffer layer. Furthermore, as described below, Ek et al. teach away from using the stepped buffer layer in the Description of the Invention section of their patent.

Applicants also note that Kusuda et al. disclose a P-I-N diode structure in which the intrinsic GaAs layer serves as the active layer of the laser structure. The present invention as recited in claims 1 and 3 uses the stacked AlGaAs layers, all either P-type or N-type, and, thus, does not include an intrinsic GaAs layer in the recited npnp thyristor structure.

Furthermore, neither Kusuda et al, Uchida or Ek disclose or suggest a configuration in which AlGaAs is used as the stepped layer and the concentration of Al is increased in each layer, as required by claim 1. Ek discloses only an SiGe stepped buffer layer (see col. 1, lines 38-42) and this layer is disclosed only in the Background section of the patent. In the Description of the Invention, Ek teaches that this stepped layer is not needed as long as thin layers of Si and SiGe are used. In the Uchida reference, the stepped layer is always InGaAs (see col. 4, lines 31-37). Kusuda does not disclose or suggest the use of any stepped layer. The buffer layer used by Kusuda is an n-type GaAs layer. (See col. 22, lines 15 and 16).

Furthermore, even if the references are combined they do not produce the subject invention. Kusuda discloses four unstepped AlGaAs layers formed on an un-stepped GaAs buffer layer. Ek, at most, discloses a stepped SiGe buffer layer and also teaches away from using a stepped buffer layer. Uchida also discloses a stepped buffer layer but Uchida's buffer layer is formed from InGaAs. None of these references either alone or in combination discloses or suggests 1) forming the stepped or graded layer as the first layer on top of the buffer layer or 2) forming the stepped or graded layer from AlGaAs, where the Al composition is increased in steps upward from the buffer layer.

The present invention, as recited in claim 3, contains a similar feature which is neither disclosed, nor suggested by the Kusuda et al., Uchida and Ek et al., singly or in combination, namely:

...four layers consisting of a first conductivity type of AlGaAs layer and a second conductivity type of AlGaAs layer stacked alternately on the buffer layer;

wherein the Al composition of the AlGaAs layer just above the buffer layer is increased upward continuously. (Emphasis Added)

Therefore, for the reasons set forth above, claims 1 and 3 are not subject to rejection under 35 USC §103(a) as being unpatentable over Kusuda et al. in view of Uchida and Ek et al.

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As claims 12-17, as amended, depend from any one of independent claims 1, 3, or 5, these claims are not subject to rejection as well. Applicants appreciate the indication in the Office Action that claims 2 and 4 are objected to as being dependent on a rejected claim and would be allowed if amended to include all of the limitations of their base claims. Because claims 1 and 3 are not subject to rejection, for the reasons set forth above, claims 2 and 4 which depend from claims 1 and 3 are not subject to rejection.

# CONCLUSION

Based on the foregoing amendment and remarks, Applicants respectfully submit that claims 1-4 and 12-17, as amended, are in condition for allowance. Accordingly, reconsideration and allowance of all pending claims are respectfully requested.

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, with sufficient postage, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on:

Respectfully submitted,

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